ECR #: 44

Title: 3.3V VDDQ_{min} Change

Release Date: 4/1/98

Impact: Change

Spec Version: A.G.P. 1.0

Summary: AGP 1.0 ECR #23 states that the VDDQ voltage during 3.3V operation must be 3.15V to 3.45V. This ECR changes 3.3V VDDQ_{min} to 3.1V. *This will NOT change the tolerance on VCC. It also does not change VDDQ tolerance at 1.5V.*

Background:

AGP 2.0 requires that a "flexible" voltage regulator is placed on the motherboard. This regulator must be able to deliver 3.3 volts if a 3.3 volt card is placed in the system (TYPEDET# floating) or 1.5 volts if a 1.5 volt card is placed in the system (TYPEDET# grounded).

The current specification (as of ECR #23) gives 150mV of tolerance (3.3V - 3.15V). The 3.3V output from a standard ATX power supply has a tolerance of +/- 4% (132mV). This means that it is not possible to regulate VDDQ from the 3.3V output of an ATX power supply (as only 18mV of drop is acceptable).

It is possible to regulate the 5 volt output of the ATX power supply to VDDQ, however this solution requires a more expensive switching regulator. The issue with a linear regulator arises during 1.5 volt operation. The voltage drop across the regulator is 3.5V (5V - 3.5V; it could be slightly higher due to the tolerance of the 5 volt supply and the regulator). At 2 amps, a 3.5 volt drop requires a linear regulator capable of dissipating 7 watts (requiring a heatsink).

Changing VDDQ_{min} to 3.1V will provide 200mV of tolerance (of which 132mV is used by the ATX power supply). This leaves 68mV of drop for the voltage regulator. This can be accomplished using a FET with Rds_{on} in the $20\text{--}30m\Omega$ range. Further VDDQ generation/delivery recommendations will be provided in the AGP Design Guide.

Change Current Specification as shown:

AGP 1.0 Interface Specification; ECR23

Current:

Table 4-1: DC Specifications for A.G.P. 1X Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vddq	I/O Supply Voltage		3.15	3.45	V	1
V _{ih}	Input High Voltage		0.5Vddq	Vddq+0.5	V	
V _{il}	Input Low Voltage		-0.5 0.3Vddq		V	
l _{il}	Input Leakage Current	0 < V _{in} < Vddq		±10	μΑ	
V _{oh}	Output High Voltage	I _{out} = -500 μA	.9Vddq		V	
V _{ol}	Output Low Voltage	I _{out} = 1500 μA		.1Vddq	V	
C _{in}	Input Pin Capacitance			8	pF	2
C _{clk}	CLK Pin Capacitance		5	12	pF	
V _{ol}	Output Low on OVRCNT#	$I_{out} = \pm 20 \mu A$		0.4	V	
V _{oh}	Output High on OVRCNT#	$I_{out} = \pm 20 \mu A$	2.4	3.6	V	

Table 4-12: Add-in Card Power Supply Limits

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vddq1.5	I/O Supply Voltage	$I_{MAX} = 8.0 \text{ A}$	1.425	1.575	V	1
Vddq3.3	I/O Supply Voltage	$I_{MAX} = 8.0 \text{ A}$	3.15	3.45	V	1
VCC3.3	3.3 V Power Supply	$I_{MAX} = 6.0 \text{ A}$	3.15	3.45	V	
VCC5	5 V Power Supply	$I_{MAX} = 2.0 \text{ A}$	4.75	5.25	V	
VCC12	12 V Power Supply	$I_{MAX} = 1.0 \text{ A}$	11.4	12.6	V	

Change:

Table 4-1: DC Specifications for A.G.P. 1X Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vddq	I/O Supply Voltage		3.1	3.45	V	1, 5
V _{ih}	Input High Voltage		0.5Vddq	Vddq+0.5	V	
V _{il}	Input Low Voltage		-0.5	0.3Vddq	V	
l _{il}	Input Leakage Current	$0 < V_{in} < Vddq$		±10	μА	
V _{oh}	Output High Voltage	I _{out} = -500 μA	.9Vddq		V	
V _{ol}	Output Low Voltage	I _{out} = 1500 μA		.1Vddq	V	
C _{in}	Input Pin Capacitance			8	pF	2
C _{clk}	CLK Pin Capacitance		5	12	pF	
V _{ol}	Output Low on OVRCNT#	$I_{out} = \pm 20 \mu A$		0.4	V	
V _{oh}	Output High on OVRCNT#	$I_{out} = \pm 20 \mu A$	2.4	3.6	V	

Notes:

Table 4-3: Add-in Card Power Supply Limits

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vddq1.5	I/O Supply Voltage	$I_{MAX} = 8.0 \text{ A}$	1.425	1.575	V	1
Vddq3.3	I/O Supply Voltage	$I_{MAX} = 8.0 \text{ A}$	3.1	3.45	V	1
VCC3.3	3.3 V Power Supply	$I_{MAX} = 6.0 \text{ A}$	3.15	3.45	V	
VCC5	5 V Power Supply	$I_{MAX} = 2.0 \text{ A}$	4.75	5.25	V	
VCC12	12 V Power Supply	$I_{MAX} = 1.0 \text{ A}$	11.4	12.6	V	

^{5.} The VDDQ voltage regulator can take advantage of the asymmetrical VDDQ tolerance when generating VDDQ. The $VDDQ_{min}$ change allows VDDQ regulation using the 4% 3.3V ATX output and a linear regulator. Refer to the Design Guide for more information on AGP power delivery. NOTE: 1.5V VDDQ maintains a symmetrical voltage tolerance.